

FIG. 2A

200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		S/P	Unit	ALUopcode CMPcc				0				CC	Rx				Rxe				Ry				0	Ccombo				Dpack	

FIG. 2B

202

204	CC	Description	C-N-V-Z Setting
	Z(EQ)	Zero or Equal	Z=1
	NZ(NE)	Not Zero or Not Equal	Z=0
	HI	Higher (unsigned)	(C=1)&&(Z=0)
	HS(CS)	Higher or Same (unsigned, or Carry Set)	C=1
	LO(CC)	Lower (unsigned, or Carry Clear)	C=0
	LS	Lower or Same (unsigned)	(C=0) (Z=1)
	VS	Overflow Set	V=1
	VC	Overflow Clear	V=0
	POS	Positive	(N=0)&&(Z=0)
	NEG	Negative	N=1
205	GE	Greater-than or Equal (signed)	N=V
206	GT	Greater-Than (signed)	(Z=0)&&(N=V)
207	LE	Less-than or Equal (signed)	(Z=1) (N!=V)
208	LT	Less-Than (signed)	N!=V

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FIG. 3A

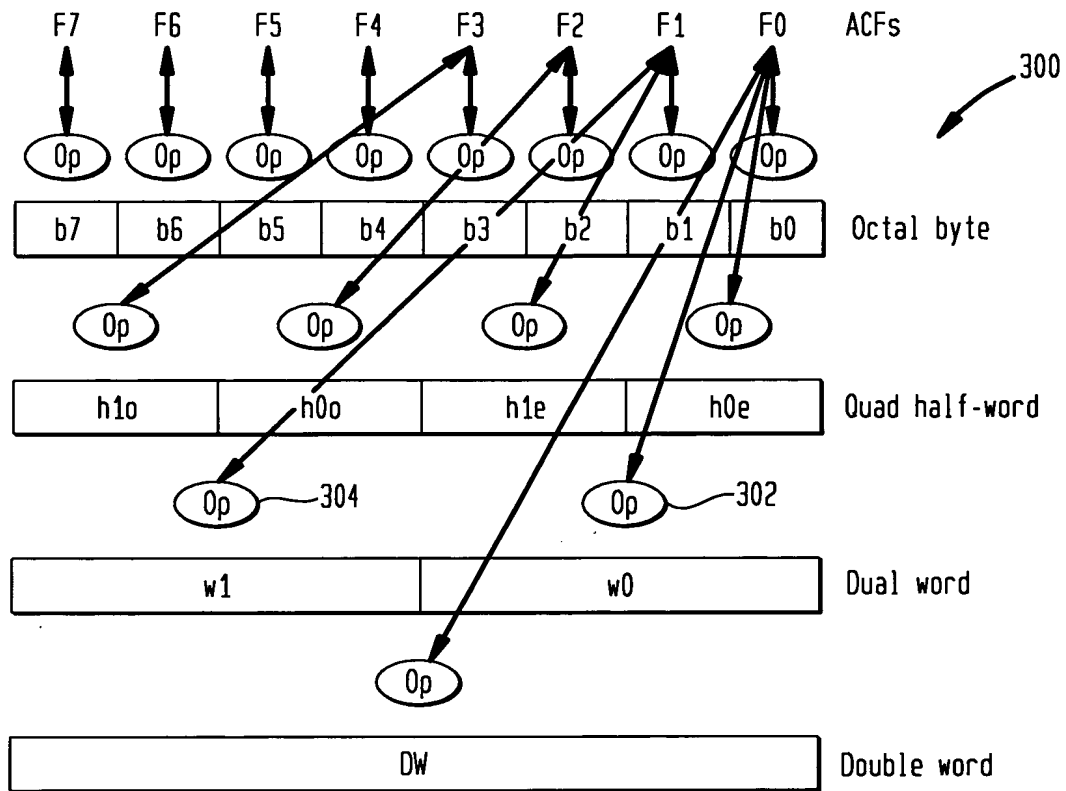


FIG. 3B

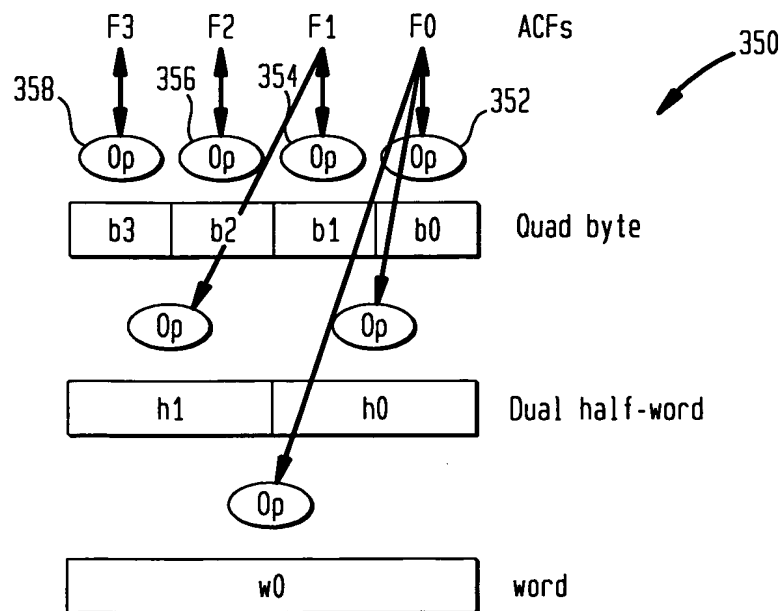


FIG. 4A

Load Direct Instruction Encoding																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		S/P		Size		0		Amode		Load		CE1		Rt 5-0		L/S		UADDR15													

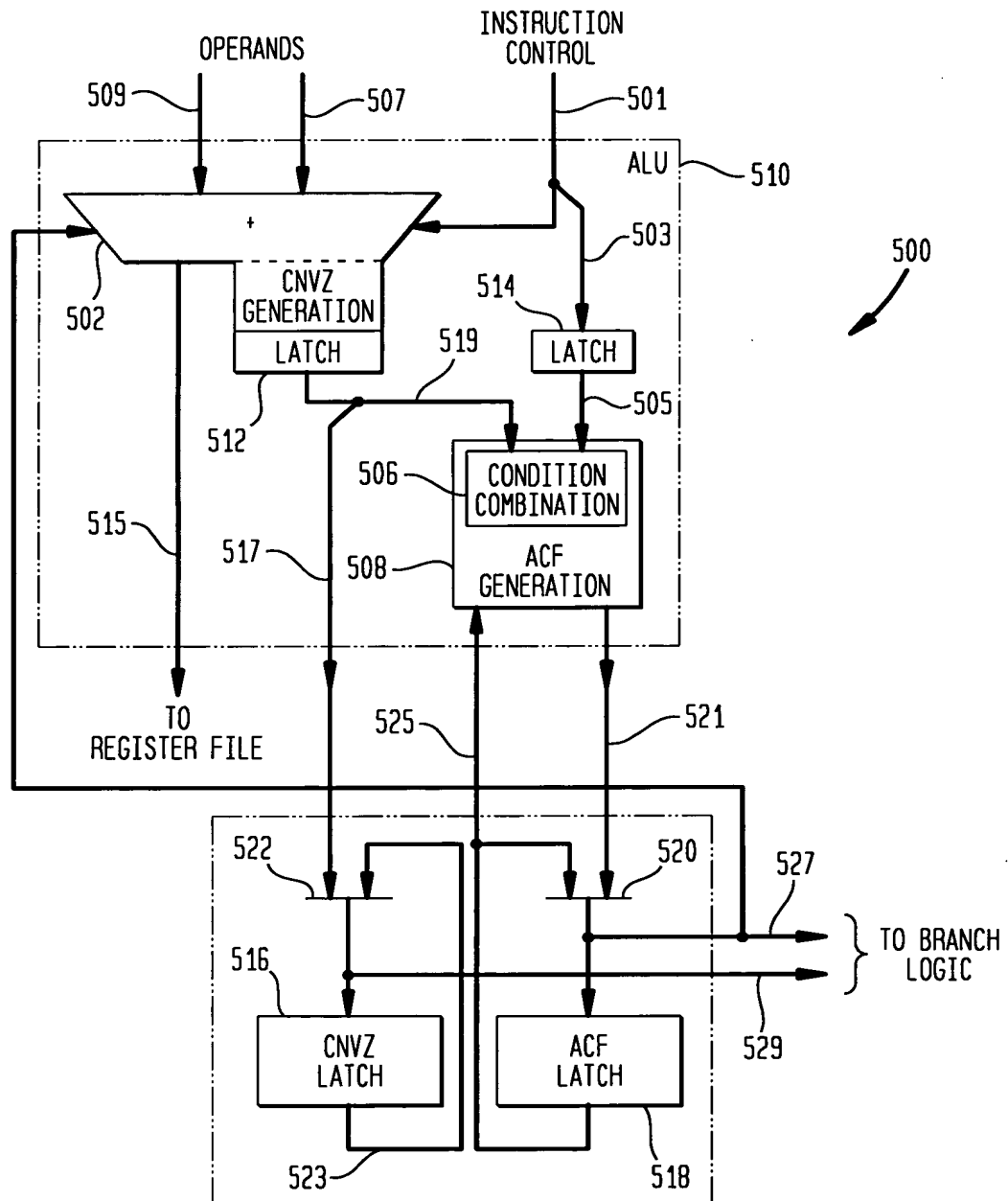
FIG. 4B

Copy Instruction Encoding																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group		S/P		Size		DSUopcode		Copy		Rt 4-0		Rx 4-0		Rt 5		Rx 5		CopyExt		CE2											

FIG. 4C

Logic Instruction Encoding																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<u>Group</u>		<u>S/P</u>		<u>Unit</u>		<u>ALUopcode</u>		<u>Logic Operation</u>		<u>Rt</u>		<u>Rx</u>		<u>Ry</u>		<u>Rte</u>		<u>Rxe</u>		<u>Rye</u>		<u>CE3b</u>		<u>LogicExt</u>							

FIG. 5A



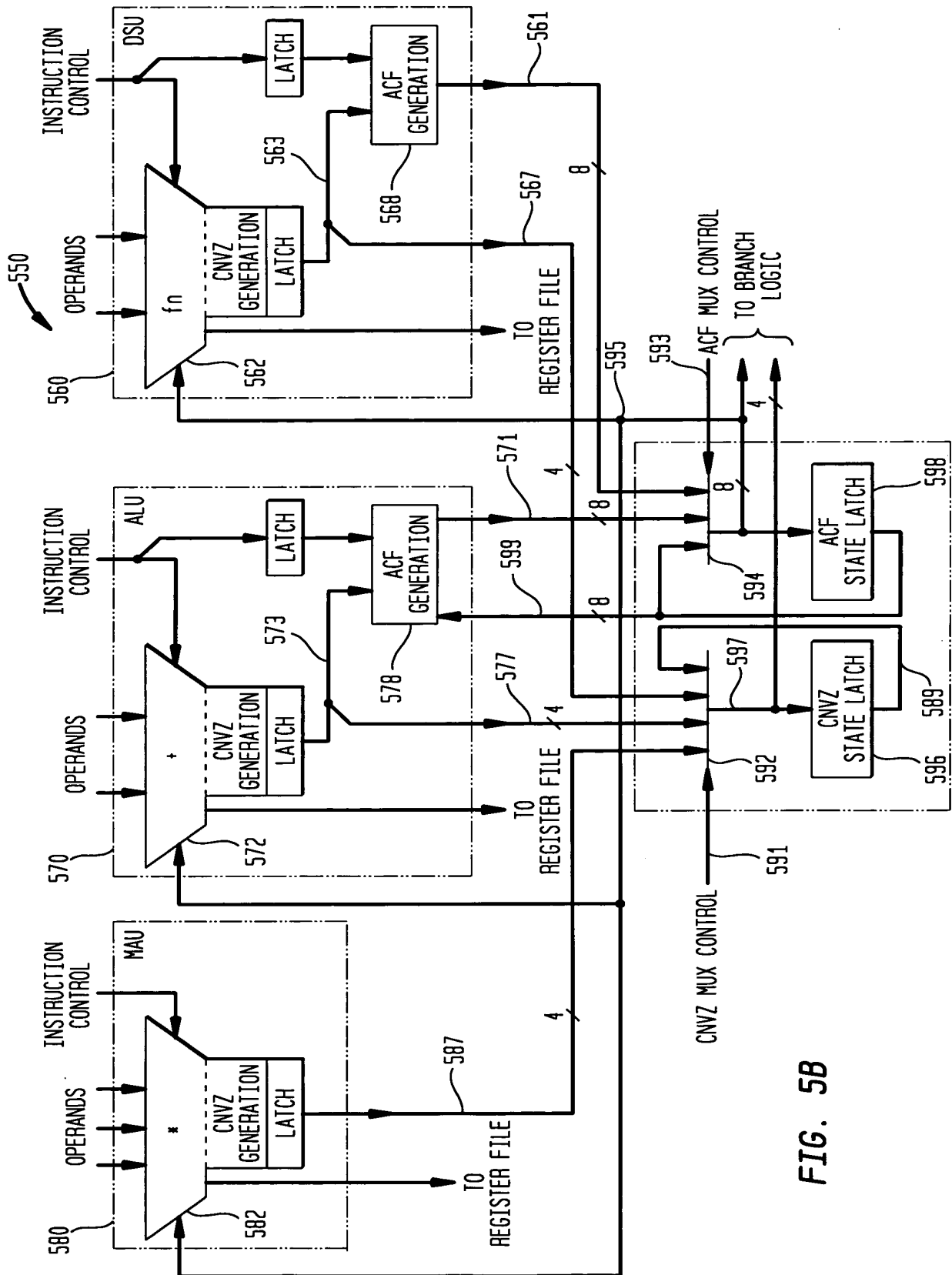


FIG. 5B